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6. AUTHOR(S)

Ian Gallimore

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Commander
Naval Air Warfare Center Aircraft Division
22541 Millstone Road
Patuxent River, Maryland 20670-5304

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

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13. ABSTRACT (*Maximum 200 words*)

The MIL-STD-1553 interface provides a reliable, high speed data interchange protocol for electronic systems. A typical 1553 bus architecture for avionics is shown in figure 1. A central processor, or mission computer, uses multiple independent 1553 channels, in this case two channels, each of which is dual redundant. Typical functions of the MC are: (1) acting as the bus controller (BC) for all 1553 channels; (2) integrating data from the various sensors to calculate navigation and fire control solutions; and (3) generating display information for the pilot.

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Enclosure (5)

The MIL-STD-1553 interface provides a reliable, high speed data interchange protocol for electronic systems. A typical 1553 bus architecture for avionics is shown in Figure 1. A central processor, or mission computer (MC), uses multiple independent 1553 channels, in this case two channels, each of which is dual redundant. Typical functions of the MC are: 1) acting as the bus controller (BC) for all 1553 channels; 2) integrating data from the various sensors to calculate navigation and fire control solutions; and 3) generating display information for the pilot. A more advanced architecture provides two MCs, which communicate on three or more channels, and which pass bus controller duty for each channel back and forth depending on operating mode; this also provides for some redundancy of MC functions. After extensive testing, the MC software is typically upgraded in the field via a portable program loader.

Remote Terminals (RTs) found in aircraft applications include the Inertial Navigation System (INS), Flight Control Computer (FCC), Radar, Instrument Landing System (ILS), Data Link (DL) radio, Weapons Management Computer (WMC), and Multi-Function Displays (MFDs). Each RT is capable of sending 30 sub-addresses and receiving 30 sub-addresses, each containing up to 32 16-bit words (64 bytes). An average RT will use about half of the available data capacity (each way), though some data-intensive RTs may approach the limit (MFDs, for example).

Most RTs are polled periodically by the MC. (In 'polling' we include BC to RT transfers, or receive commands.) Individual sub-addresses are polled repeatedly to provide an updated stream of dynamic data. Cycle rates vary according to function, and common rates are 20Hz, 5Hz, and 1Hz; some transfers may be requested 'on demand' at any rate up to some maximum predetermined rate, e.g., 100Hz, though this type of scheduling is unusual. Typical 1Hz data may include equipment status or Built-In-Test (BIT) data, while 5Hz data may include, for example, a frequency setting for a radio, or a mode control for a radar. At 20Hz, the MC polls for INS measurements such as vehicle altitude, acceleration, and attitude, and sends them to the FCC for use in the automatic pilot calculations. This amounts to an effective data rate of about 20kbps, excluding overhead. MFDs are also usually updated at 20Hz. A mature aircraft system may contain many more RTs, all operating simultaneously at relatively high update rate, so bus loading of a particular channel can approach 80-90% of capacity in some applications.

One useful RT function is the 'memory inspect'. During memory inspect, the MC sends to the RT a sub-address which contains a base address and word count. The RT replies with the requested number of words, starting from the indicated base address in memory. The MC displays the results, providing more detailed on-line troubleshooting information to the maintenance technician, test engineer, or operator. Note that this function requires a fixed and published map of the RTs internal memory.

In some applications the designer may need to synchronize transfers between the BC and RT. For example, a display device may send keypress data from the pilot to the MC, while the MC sends display data back to the device. Unpredictable operation can result without synchronization. Synchronization can be done using 1553 mode codes: one mode code indicates to the RT when to start processing new display data from the MC, and another indicates to the RT when the keypress data has been read. Keypress data is buffered in the RT and then clocked out using the second mode code, so that predictable operation is assured.

One recent system we have built utilizes BC, RT, and monitor terminal (MT) capabilities simultaneously to provide a means to test prototype navigation sensors and displays using existing MC and display interfaces. Figure 2 illustrates the use of a 'bypass computer' which is inserted in the 1553 bus between the MC and an existing RT (the ILS receiver). The existing RT is controlled by the bypass computer, while the bypass computer acts as an RT and supports the existing interface to the MC. The prototype sensor provides data to the bypass computer, which also monitors the INS data. In flight, the pilot is able to select either system using a software data switch internal to the bypass computer. In the 'normal mode', the existing RT's data is passed straight through the bypass

computer. In the 'emulation mode', data from the prototype system is blended with the INS data, and the solution is routed to the existing interface with the MC, while the data from the existing RT is not used. This system has been tested successfully in a hardware-in-the-loop test environment, and is currently being prepared for flight testing. The system is housed in a rugged 1/2 ATR-Short VME chassis containing a single board computer with 1553 interface, and a dedicated 1553 interface card (among others). A real-time kernel with fast context switching is used to minimize data latency across the bypass computer.

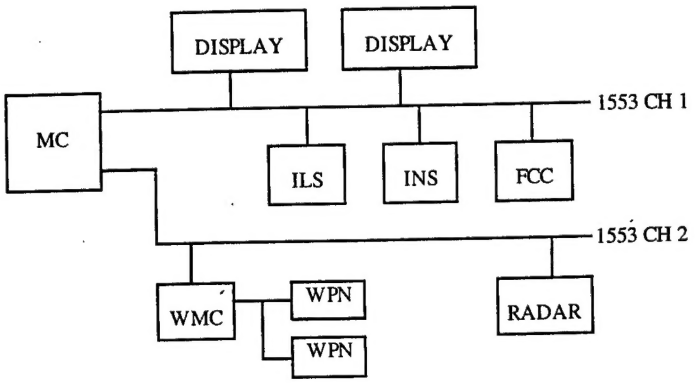

Figure 1 - Typical
Avionics Architecture

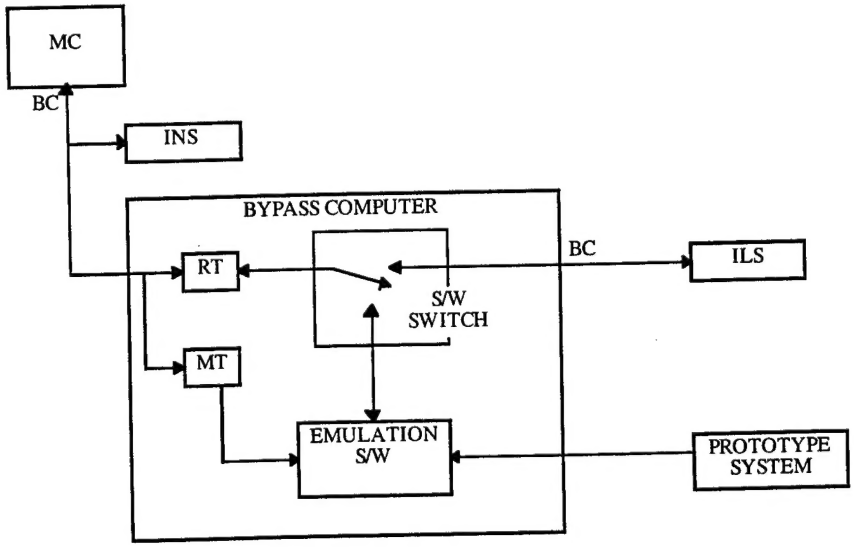

Figure 2 - Use of BC, RT,
MT for Prototype Testing

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bio stuff:

Ian Gallimore is a Senior Project Engineer at the Naval Air Warfare Center Aircraft Division in Patuxent River, MD. He is responsible for advanced system design and product development and can be reached via email at GallimoreIT%am4@mr.nawcad.navy.mil. He enjoys his wife's poetry and playing bad left-handed golf with his kids.